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CLAIMS

(57) [Claim(s)]

[Claim 1] The 1st and 2nd transistors by which both :drain electrodes were connected to the 1st power source in the current detector using two or more FET transistors, and both gate electrodes were connected to the input signal terminal;
Constant current source connected between the source electrode of said 1st transistor, and the 2nd power source;
Electrical-potential-difference comparator by which one input was connected to the source electrode of said 1st transistor, and the input of another side was connected to the source electrode and output terminal of said 2nd transistor;
The current detector characterized by detecting stably an excess of a predetermined value of the output current which flows said output terminal by comparing the potential of a preparation and the source electrode of said 2nd transistor with the potential of the source electrode of said 1st transistor.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to a current detector. It is the circuit which used power metal-oxide semiconductor field effect transistor for the detail more, and is related with the highly precise current detector which detects that the output current exceeded the maximum allowed value, and intercepts MOSFET.

[0002]

[Description of the Prior Art] Conventionally, there was a circuit as shown in drawing 1 as a current detector the voltage regulator using power metal-oxide semiconductor field effect transistor, and for Motor Driver. two juxtaposition n channel MOS FET transistors M1 which made the current detector 10 in the monolithic device as shown in this drawing, and M2 from -- it changes. MOSFET transistor M1 for detection which is the 1st transistor A drain electrode is the output current (load current) I_o . Output terminal Po to receive Connecting, a gate electrode is the input signal terminal V_g . Connecting, a source electrode is the monitor resistance R_m . It minds and connects with the ground. Power-metal-oxide-semiconductor-field-effect-transistor transistor M2 which is the 2nd transistor Transistor M1 A drain electrode is an output terminal Po similarly. It connects and a gate electrode is the input signal terminal V_g . It connects. Transistor M2 The source electrode is directly connected to the ground. Thus, the output current I_o By dividing into the power section and a detecting element, it is the monitor resistance R_m .

It carries out to detection and has come to be able to carry out insertion use. The current detector 10 has the electrical-potential-difference comparator COMP again. The non-inversed input terminal of the electrical-potential-difference comparator COMP is the 1st transistor M1. A source electrode and monitor resistance Rm The node of a between to electrical potential difference Vm It inputs. The inversed input terminal of the electrical-potential-difference comparator COMP inputs reference voltage Vrf from the positive electrode of the source of reference voltage where the negative electrode was grounded. [0003] Below, actuation of the current detector 10 is explained. Generally, it is the drain current Id of MOSFET. Vds is expressed with a degree type in approximation in a very small active region compared with Vgs.

[0004] $I_d = K \cdot W/L \cdot (V_{gs} - V_{th}) V_{ds}$ -- for a proportionality constant and W/L, the width versus length of a channel and Vgs are [K / threshold voltage and Vds of the electrical potential difference between the gate sources and Vth] the electrical potential differences between the drain sources here.

[0005] Monitor resistance Rm When it assumes that a value is sufficiently small, it is a transistor M1. Current I1 which flows when it is ON Rm to depend The value for a voltage drop Vm (= I1 and Rm) is a transistor M1. It can ignore compared with ON state voltage Vds between the drain sources. When this condition is fulfilled, it sets at an upper ceremony and is both the FET transistor M1 and M2. It can consider that Vds(es) and Vgs(es) are equal respectively. Since it can consider that both the transistors M1 and the threshold voltage Vth of M2 are almost equal, it is the FET transistor M2. Drain current I2 FET transistor M1 Drain current I1 A ratio I_2 / I_1 It is set to $I_2 / I_1 = (W_2 / L_2) / (W_1 / L_1) = n$, and becomes fixed. Therefore, it is I1 if mirror ratio n is known. By detecting a value, the value of I2 (= n·I1), therefore Io (= (n+1) and I1) can be known. It is good as a value of n at 1000.

[0006] Io I1 I1 since it can consider that it is in proportionality Monitor resistance Rm to depend A part for a voltage drop Vm It compares with reference voltage Vrf (refer to drawing 2), and is Vm. By detecting having exceeded reference voltage Vrf, it is Io. It is detectable to have exceeded the predetermined value. In the current detector 10 of drawing 1 , it is Vm. If reference voltage Vrf is exceeded, Comparator COMP is the current-limiting signal Co. It outputs (refer to drawing 2). Current-limiting signal Co By being outputted, it is the output current Io. It is detectable to have exceeded the predetermined value. Current-limiting signal Co For example, gate voltage Vg By inputting in the current-limiting circuit (not shown) to control, it is gate voltage Vg. It can be made zero and the MOSFET transistor M1 and M2 can be intercepted.

[0007] as mentioned above, proper precision with the comparatively good division current which flows between MOSFETs by which on resistance was adjusted within the monolithic device -- **** -- since it is, the power-metal-oxide-semiconductor-field-effect-transistor current detector 10 enables measurement of the load current of a power equalization circuit etc. somewhat efficiently. Monitor resistance Rm It is Rm if it is 10 or less % of the on resistance of the detecting-element transistor M1. Current I1 which can be disregarded and is detected It becomes the output current / current mirror ratio, i.e., I_2 / n , mostly.

[0008]

[Problem(s) to be Solved by the Invention] However, in fact, it is the detecting-element transistor M1 in order to suppress detection loss low. Channel width W1 Transistor M2

W2 It must compare and must design small ($W1 \ll W2$). In that case, transistor M1 It compares with on resistance and is R_m . If it is made small to extent which can be disregarded, it is the resistance R_m for detection. It becomes inadequate [the generated electrical potential difference for detection] for usually driving the current-limiting circuit containing a comparator etc. Therefore, it cannot but stop using a to some extent big value for R_m , and is R_m . It becomes impossible to ignore. Then, the sum total resistance by the side of detection (mirror) swells up considerably, and there is a trouble that current mirror ratio will change. Namely, R_m If it cannot ignore, it is a transistor M1. M2 The electrical potential difference V_{ds} between the drain sources becomes mutually equal less, current mirror ratio is out of order by this, and detection precision worsens. [0009] This invention aims at offering the current detector where detection precision is high in view of the above troubles.

[0010] Other purposes of this invention are offering a current detector without detection loss, without using the output current in a monitor circuit.

[0011]

[Means for Solving the Problem] Current detector 30 using two or more FET transistors which can be set to this invention in order to attain the above-mentioned purpose: Both drain electrodes are connected to the 1st power source V_{dd} . Both gate electrodes are the input signal terminals V_g . The 1st and 2nd connected transistors M1, M2 **; The 1st transistor M1 Constant current source I_{rf} connected between a source electrode and the 2nd power source (ground); one input -- the 1st transistor M1 It connects with a source electrode. The input of another side is the 2nd transistor M2. Electrical-potential-difference comparator COMP connected to the source electrode and the output terminal; It has. The 2nd transistor M2 The potential and the 1st transistor M1 of a source electrode The output current I_o which flows an output terminal by comparing the potential of a source electrode It is characterized by detecting an excess of a predetermined value.

[0012]

[Function] In the current detector of this invention constituted as mentioned above Both transistors M1 and M2 Both the source potential V_1 and V_2 When exactly equal ($V_1 = V_2$), it is the ratio I_2 of the drain current of both transistors / I_1 . It operates so that it may be set to $I_2 / I_1 = (W_2 / L_2) / (W_1 / L_1) = n$ (mirror ratio). In order that I_1 may take a predetermined value according to a constant current source I_{rf} , it is output current $I_o = I_2$. It will be set to $I_2 > I_1$ and n if it flows exceeding the maximum allowed current value I_{mx} . Then, V_2 It falls and is $V_1 > V_2$. The comparator COMP which became and detected it is the current-limiting signal Co . It outputs.

[0013]

[Example] The example of this invention is explained with reference to a drawing below. Drawing 3 shows the configuration of the current detector which is one example of this invention. two juxtaposition n channel MOS FET transistors M1 which made the current detector 30 in the monolithic device as shown in this drawing, and M2 from -- it changes. A transistor M1 and M2 A p channel may be used by circuitry as shown in drawing 5 , and you may be MOSFET of other formats. MOSFET transistor M1 for detection which is the 1st transistor A drain electrode is connected to supply voltage V_{dd} , and a gate electrode is the input signal terminal V_g . It connects and the source electrode is connected to the ground which is the 2nd power source through the constant current source I_{rf} . Power-metal-oxide-semiconductor-field-effect-transistor transistor M2 which

is the 2nd transistor Transistor M1 Similarly, a drain electrode is connected to supply voltage Rhine Vdd, and a gate electrode is the input signal terminal Vg. It connects. Transistor M2 A source electrode is the output current (load current) Io. Output terminal Po to take out It connects. Thus, it sets to this invention and is the output current Io. It is not dividing into the power section and a detecting element. Therefore, a detecting element affects an output side. The current detector 30 has the electrical-potential-difference comparator COMP again. The non-inversed input terminal of the electrical-potential-difference comparator COMP is the 1st transistor M1. The node between a source electrode and a constant current source Irf to electrical potential difference V1 It inputs. the inversed input terminal of the electrical-potential-difference comparator COMP -- output terminal Po from -- electrical potential difference V2 It inputs. The electrical-potential-difference comparator COMP is the current-limiting output signal Co, if the reversal input value becomes smaller than a noninverting input value. It outputs.

[0014] Below, actuation of the current detector 30 is explained. Because of explanation of operation, it is both the transistors M1 and M2. Both the source potential V1 and V2 It is assumed mutually that it is an equal ($V1 = V2$) thing. At this time, the electrical-potential-difference comparator COMP is the current-limiting signal Co. It does not output. Generally it is the drain current Id of MOSFET. Vds is expressed with a degree type like the above-shown in a very small active region compared with Vgs.

[0015] $I_d = K \cdot W/L \cdot (V_{gs} - V_{th}) V_{ds}$ By the $-(V_{gs} - V_{th})$ Vds above-mentioned assumption ($V1 = V2$), it is both the transistors M1 and M2. Electrical-potential-difference Vds(es) between the drain sources and electrical-potential-difference Vgs(es) between the gate sources are equal respectively. Both the transistors M1 and M2 Since it can consider that threshold voltage Vth is almost equal, it is the FET transistor M2. Drain current I2 FET transistor M1 The ratio I2 with the drain current I1 / I1 It is set to $I2 / I1 = (W2 / L2) / (W1 / L1) = n$. Thus, it is I1 when it shall operate according to mirror ratio n. By getting to know a value, the value of I2 ($=n \cdot I1$), therefore Io ($=I2 = n \cdot I1$) can be known. It is good as a value of n at 1000.

[0016] Thus, both the source potential V1 and V2 It is Io when equal. I1 Proportionality changes and it is *****. However, it is I1 by the constant current source Irf in fact. A predetermined value is taken. The output current Io, i.e., I2, A maximum allowed current value is set to Imx, and the current value of a constant current source Irf is set up with Imx/n . By doing so, it is I2. It is I1 when it flows exceeding Imx. Since it is still Irf ($=Imx/n$), it is set to $I2 > I1$ and n. Then, $I2 = n \cdot I1$ Proportionality collapses and it is V2. It falls and is $V1 > V2$. It becomes. The comparator COMP which detected it is the current-limiting signal Co. It outputs (refer to drawing 4). Therefore, current-limiting signal Co By having been outputted, it is Io. It is detectable to have exceeded Imx. Current-limiting signal Co For example, gate voltage Vg By outputting to the current-limiting circuit (not shown) to control, it is gate voltage Vg. It is made zero and is the MOSFET transistor M1 and M2. It can intercept.

[0017]

[Effect of the Invention] This invention is the monitor resistance Rm which was experienced with the conventional technique since it was constituted as above-mentioned. The detection error to depend is avoidable, it is a high precision and the effectiveness of enabling detection/limit of the load current efficiently is acquired. Moreover, current I1 for detection in a monitor circuit It is supplied from the constant current source Irf, and is

the output current I_o . Since a part is not necessarily used, it is I_o . It is not affected, but effectiveness and precision are easy also for the design of an at best still more suitable stabilization circuit, and there is great effectiveness -- it is hard to be influenced by the service condition of a circuit.

TECHNICAL FIELD

[Industrial Application] This invention relates to a current detector. It is the circuit which used power metal-oxide semiconductor field effect transistor for the detail more, and is related with the highly precise current detector which detects that the output current exceeded the maximum allowed value, and intercepts MOSFET.

PRIOR ART

[Description of the Prior Art] Conventionally, there was a circuit as shown in drawing 1 as a current detector the voltage regulator using power metal-oxide semiconductor field effect transistor, and for Motor Driver. two juxtaposition n channel MOS FET transistors M1 which made the current detector 10 in the monolithic device as shown in this drawing, and M2 from -- it changes. MOSFET transistor M1 for detection which is the 1st transistor A drain electrode is the output current (load current) I_o . Output terminal Po to receive Connecting, a gate electrode is the input signal terminal V_g . Connecting, a source electrode is the monitor resistance R_m . It minds and connects with the ground. Power-metal-oxide-semiconductor-field-effect-transistor transistor M2 which is the 2nd transistor Transistor M1 A drain electrode is an output terminal Po similarly. It connects and a gate electrode is the input signal terminal V_g . It connects. Transistor M2 The source electrode is directly connected to the ground. Thus, the output current I_o By dividing into the power section and a detecting element, it is the monitor resistance R_m . It carries out to detection and has come to be able to carry out insertion use. The current detector 10 has the electrical-potential-difference comparator COMP again. The non-inversed input terminal of the electrical-potential-difference comparator COMP is the 1st transistor M1. A source electrode and monitor resistance R_m The node of a between to electrical potential difference V_m It inputs. The inversed input terminal of the electrical-potential-difference comparator COMP inputs reference voltage V_{rf} from the positive electrode of the source of reference voltage where the negative electrode was grounded.

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[0005] Monitor resistance R_m When it assumes that a value is sufficiently small, it is a transistor M1. Current I_1 which flows when it is ON R_m to depend The value for a voltage drop V_m ($= I_1$ and R_m) is a transistor M1. It can ignore compared with ON state voltage V_{ds} between the drain sources. When this condition is fulfilled, it sets at an upper ceremony and is both the FET transistor M1 and M2. It can consider that $V_{ds}(es)$ and $V_{gs}(es)$ are equal respectively. Since it can consider that both the transistors M1 and the threshold voltage V_{th} of M2 are almost equal, it is the FET transistor M2. Drain current

I2 FET transistor M1 Drain current I1 A ratio $I2 / I1 = (W2 / L2) / (W1 / L1) = n$, and becomes fixed. Therefore, it is I1 if mirror ratio n is known. By detecting a value, the value of I2 (= n·I1), therefore Io (= (n+1) and I1) can be known. It is good as a value of n at 1000.

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[0007] as mentioned above, proper precision with the comparatively good division current which flows between MOSFETs by which on resistance was adjusted within the monolithic device -- **** -- since it is, the power-metal-oxide-semiconductor-field-effect-transistor current detector 10 enables measurement of the load current of a power equalization circuit etc. somewhat efficiently. Monitor resistance Rm It is Rm if it is 10 or less % of the on resistance of the detecting-element transistor M1. Current I1 which can be disregarded and is detected It becomes the output current / current mirror ratio, i.e., $I2 / n$, mostly.

EFFECT OF THE INVENTION

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in fact, it is the detecting-element transistor M1 in order to suppress detection loss low. Channel width W1 Transistor M2 W2 It must compare and must design small ($W1 \ll W2$). In that case, transistor M1 It compares with on resistance and is Rm. If it is made small to extent which can be disregarded, it is the resistance Rm for detection. It becomes inadequate [the generated electrical potential difference for detection] for usually driving the current-limiting circuit containing a comparator etc. Therefore, it cannot but stop using a to some extent big value for Rm, and is Rm. It becomes impossible to ignore. Then, the sum total resistance by the side of detection (mirror) swells up considerably, and there is a trouble that current mirror ratio will change. Namely, Rm If it cannot ignore, it is a transistor M1.

M2 The electrical potential difference V_{ds} between the drain sources becomes mutually equal less, current mirror ratio is out of order by this, and detection precision worsens.

[0009] This invention aims at offering the current detector where detection precision is high in view of the above troubles.

[0010] Other purposes of this invention are offering a current detector without detection loss, without using the output current in a monitor circuit.

MEANS

[Means for Solving the Problem] Current detector 30 using two or more FET transistors which can be set to this invention in order to attain the above-mentioned purpose: Both drain electrodes are connected to the 1st power source V_{dd} . Both gate electrodes are the input signal terminals V_g . The 1st and 2nd connected transistors M1, M2 **; The 1st transistor M1 Constant current source I_{rf} connected between a source electrode and the 2nd power source (ground); one input -- the 1st transistor M1 It connects with a source electrode. The input of another side is the 2nd transistor M2. Electrical-potential-difference comparator COMP connected to the source electrode and the output terminal; It has. The 2nd transistor M2 The potential and the 1st transistor M1 of a source electrode The output current I_o which flows an output terminal by comparing the potential of a source electrode It is characterized by detecting an excess of a predetermined value.

OPERATION

[Function] In the current detector of this invention constituted as mentioned above Both transistors M1 and M2 Both the source potential V_1 and V_2 When exactly equal ($V_1 = V_2$), it is the ratio I_2 of the drain current of both transistors / I_1 . It operates so that it may be set to $I_2 / I_1 = (W_2 / L_2) / (W_1 / L_1) = n$ (mirror ratio). In order that I_1 may take a predetermined value according to a constant current source I_{rf} , it is output current $I_o = I_2$. It will be set to $I_2 > I_1$ and n if it flows exceeding the maximum allowed current value I_{mx} . Then, V_2 It falls and is $V_1 > V_2$. The comparator COMP which became and detected it is the current-limiting signal C_o . It outputs.

EXAMPLE

[Example] The example of this invention is explained with reference to a drawing below. Drawing 3 shows the configuration of the current detector which is one example of this invention. two juxtaposition n channel MOS FET transistors M1 which made the current detector 30 in the monolithic device as shown in this drawing, and M2 from -- it changes. A transistor M1 and M2 A p channel may be used by circuitry as shown in drawing 5 , and you may be MOSFET of other formats. MOSFET transistor M1 for detection which is the 1st transistor A drain electrode is connected to supply voltage $R_{hine} V_{dd}$, and a gate electrode is the input signal terminal V_g . It connects and the source electrode is connected to the ground which is the 2nd power source through the constant current source I_{rf} . Power-metal-oxide-semiconductor-field-effect-transistor transistor M2 which is the 2nd transistor Transistor M1 Similarly, a drain electrode is connected to supply voltage $R_{hine} V_{dd}$, and a gate electrode is the input signal terminal V_g . It connects. Transistor M2 A source electrode is the output current (load current) I_o . Output terminal P_o to take out It connects. Thus, it sets to this invention and is the output current I_o . It is not dividing into the power section and a detecting element. Therefore, a detecting

element affects an output side. The current detector 30 has the electrical-potential-difference comparator COMP again. The non-inversed input terminal of the electrical-potential-difference comparator COMP is the 1st transistor M1. The node between a source electrode and a constant current source I_{rf} to electrical potential difference V_1 It inputs. the inversed input terminal of the electrical-potential-difference comparator COMP -- output terminal Po from -- electrical potential difference V_2 It inputs. The electrical-potential-difference comparator COMP is the current-limiting output signal Co , if the reversal input value becomes smaller than a noninverting input value. It outputs.

[0014] Below, actuation of the current detector 30 is explained. Because of explanation of operation, it is both the transistors M1 and M2. Both the source potential V_1 and V_2 It is assumed mutually that it is an equal ($V_1 = V_2$) thing. At this time, the electrical-potential-difference comparator COMP is the current-limiting signal Co . It does not output. Generally it is the drain current I_d of MOSFET. V_{ds} is expressed with a degree type like the above-shown in a very small active region compared with V_{gs} .

[0015] $I_d = K \cdot W/L$ By the $-(V_{gs} - V_{th})$ V_{ds} above-mentioned assumption ($V_1 = V_2$), it is both the transistors M1 and M2. Electrical-potential-difference $V_{ds}(es)$ between the drain sources and electrical-potential-difference $V_{gs}(es)$ between the gate sources are equal respectively. Both the transistors M1 and M2 Since it can consider that threshold voltage V_{th} is almost equal, it is the FET transistor M2. Drain current I_2 FET transistor M1 The ratio I_2 with the drain current I_1 / I_1 It is set to $I_2 / I_1 = (W_2 / L_2) / (W_1 / L_1) = n$. Thus, it is I_1 when it shall operate according to mirror ratio n . By getting to know a value, the value of I_2 ($=n \cdot I_1$), therefore I_o ($=I_2 = n \cdot I_1$) can be known. It is good as a value of n at 1000.

[0016] Thus, both the source potential V_1 and V_2 It is I_o when equal. I_1 Proportionality changes and it is *****. However, it is I_1 by the constant current source I_{rf} in fact. A predetermined value is taken. The output current I_o , i.e., I_2 , A maximum allowed current value is set to I_{mx} , and the current value of a constant current source I_{rf} is set up with I_{mx}/n . By doing so, it is I_2 . It is I_1 when it flows exceeding I_{mx} . Since it is still I_{rf} ($=I_{mx}/n$), it is set to $I_2 > I_1$ and n . Then, $I_2 = n \cdot I_1$ Proportionality collapses and it is V_2 . It falls and is $V_1 > V_2$. It becomes. The comparator COMP which detected it is the current-limiting signal Co . It outputs (refer to drawing 4). Therefore, current-limiting signal Co By having been outputted, it is I_o . It is detectable to have exceeded I_{mx} . Current-limiting signal Co For example, gate voltage V_g By outputting to the current-limiting circuit (not shown) to control, it is gate voltage V_g . It is made zero and is the MOSFET transistor M1 and M2. It can intercept.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The conventional current detector is shown.

[Drawing 2] It is a graph explaining actuation of the circuit of drawing 1 .

[Drawing 3] The current detector according to one example of this invention is shown.

[Drawing 4] It is a graph explaining actuation of the circuit of drawing 3 .

[Drawing 5] The current detector according to other examples of this invention is shown.

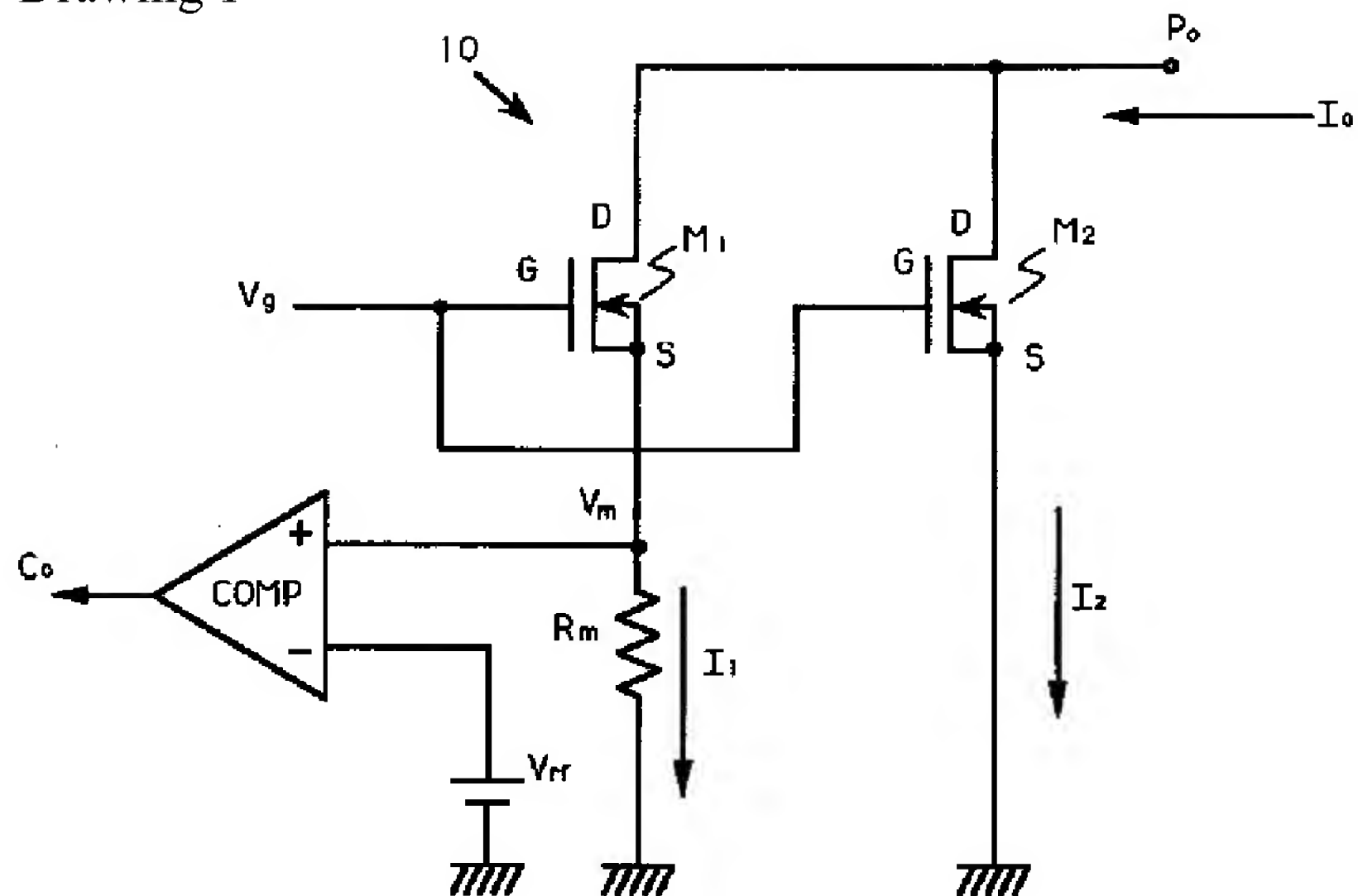
[Description of Notations]

30 Current Detector

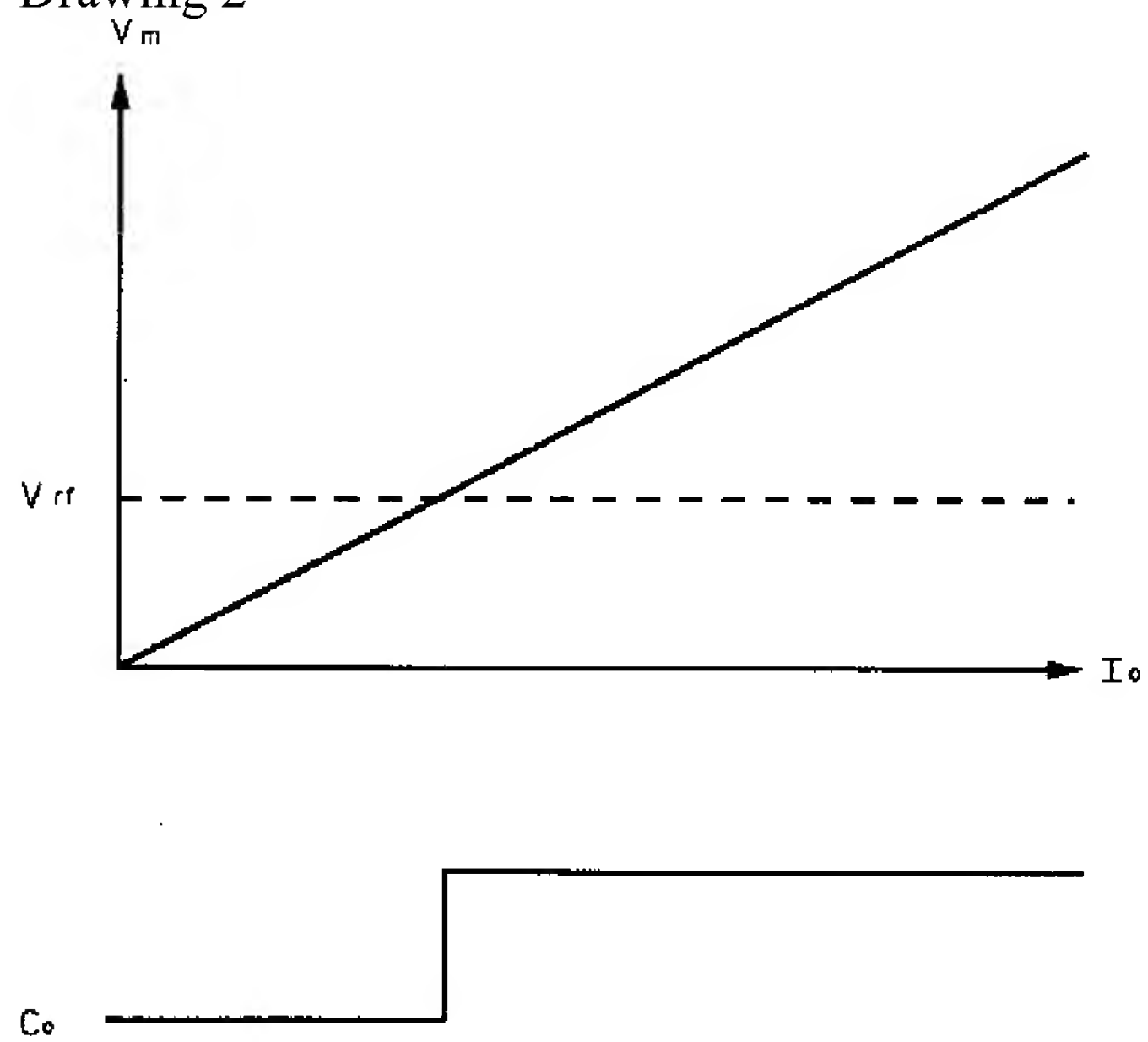
V_{dd} Supply voltage

V_g Input signal electrical potential difference
 M_1 The 1st transistor
 M_2 The 2nd transistor
 I_{rf} Constant current source
 P_o Output terminal
 $COMP$ Electrical-potential-difference comparator
 I_o Output current

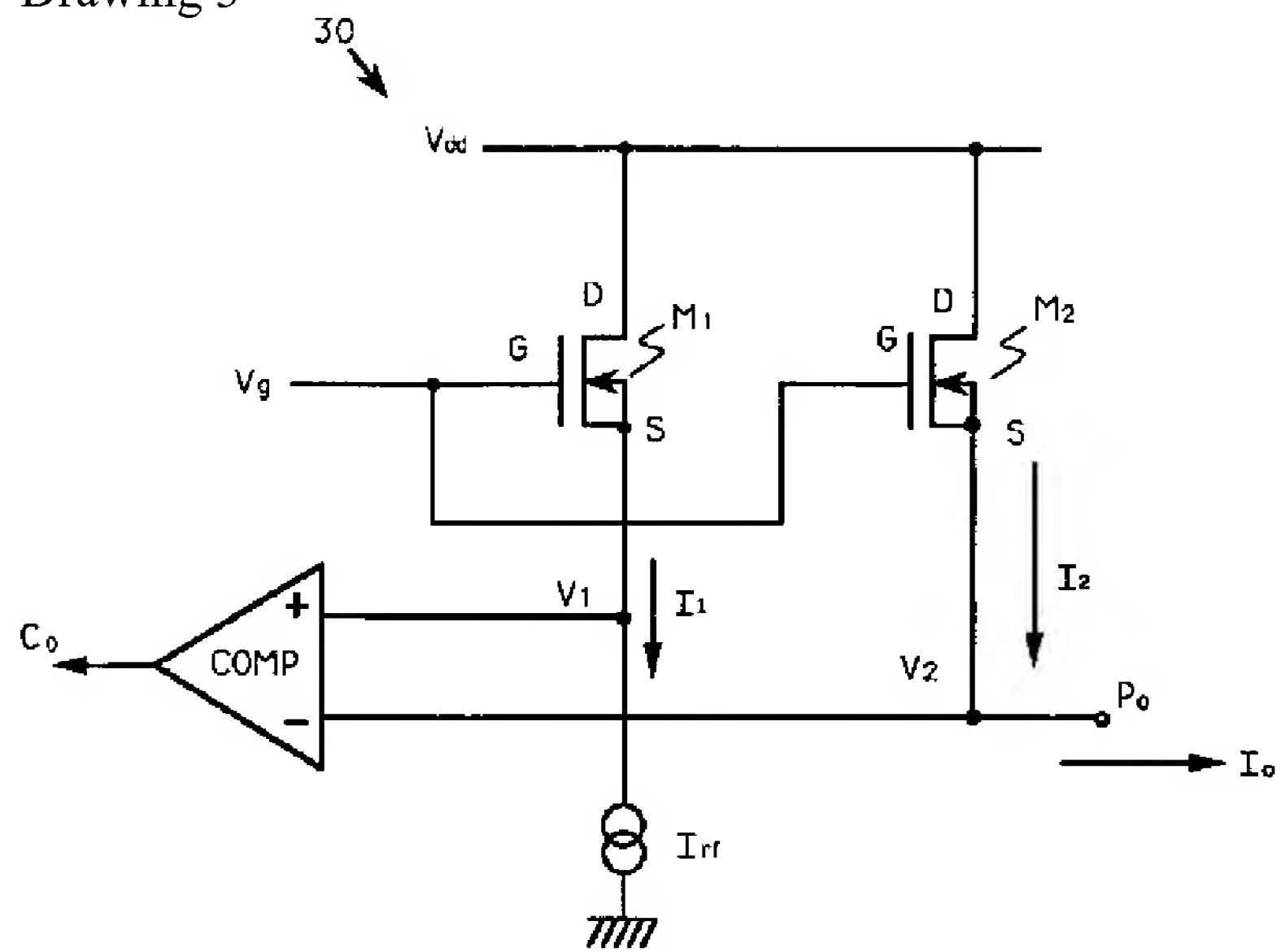
Drawing 1



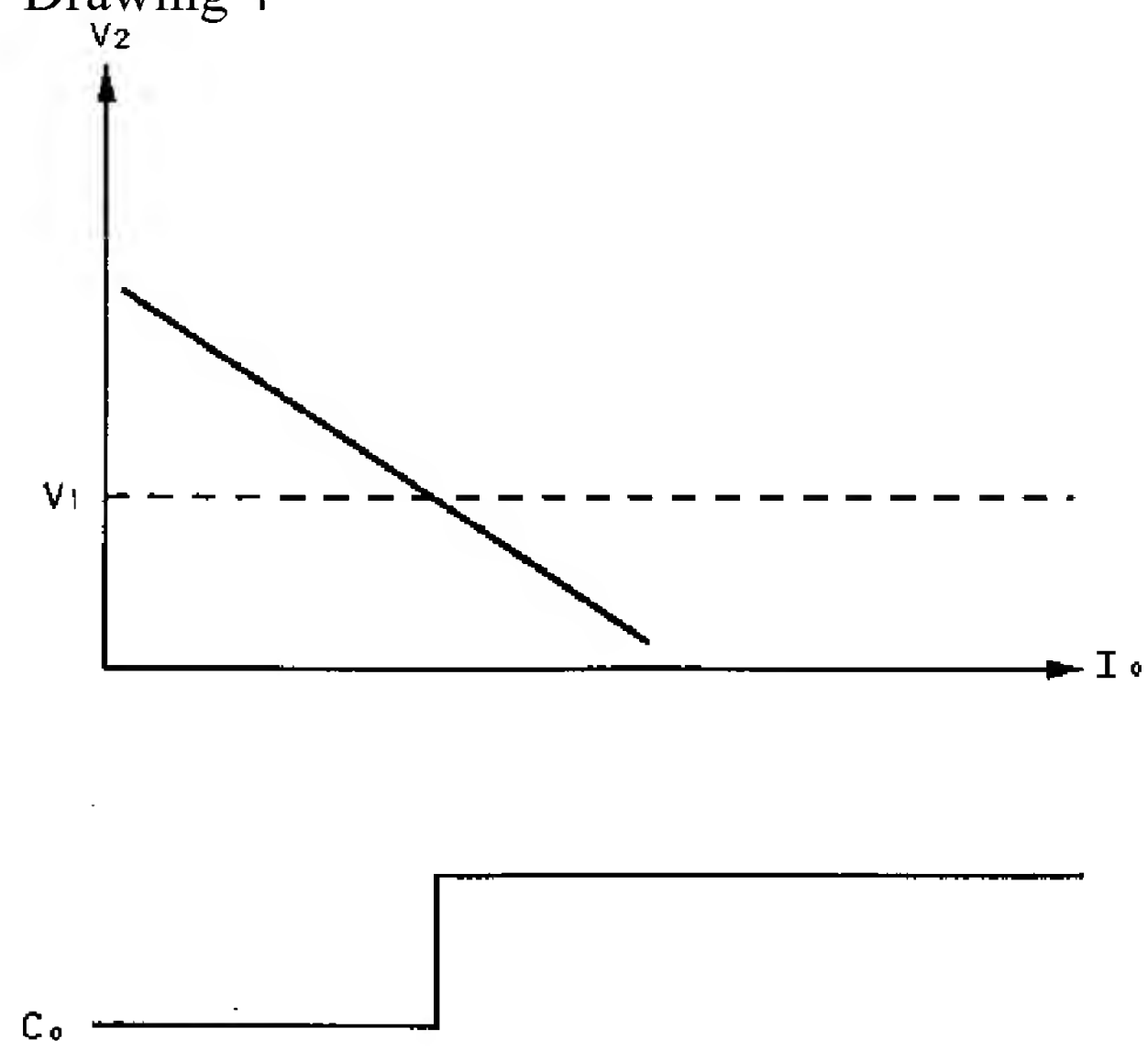
Drawing 2



Drawing 3

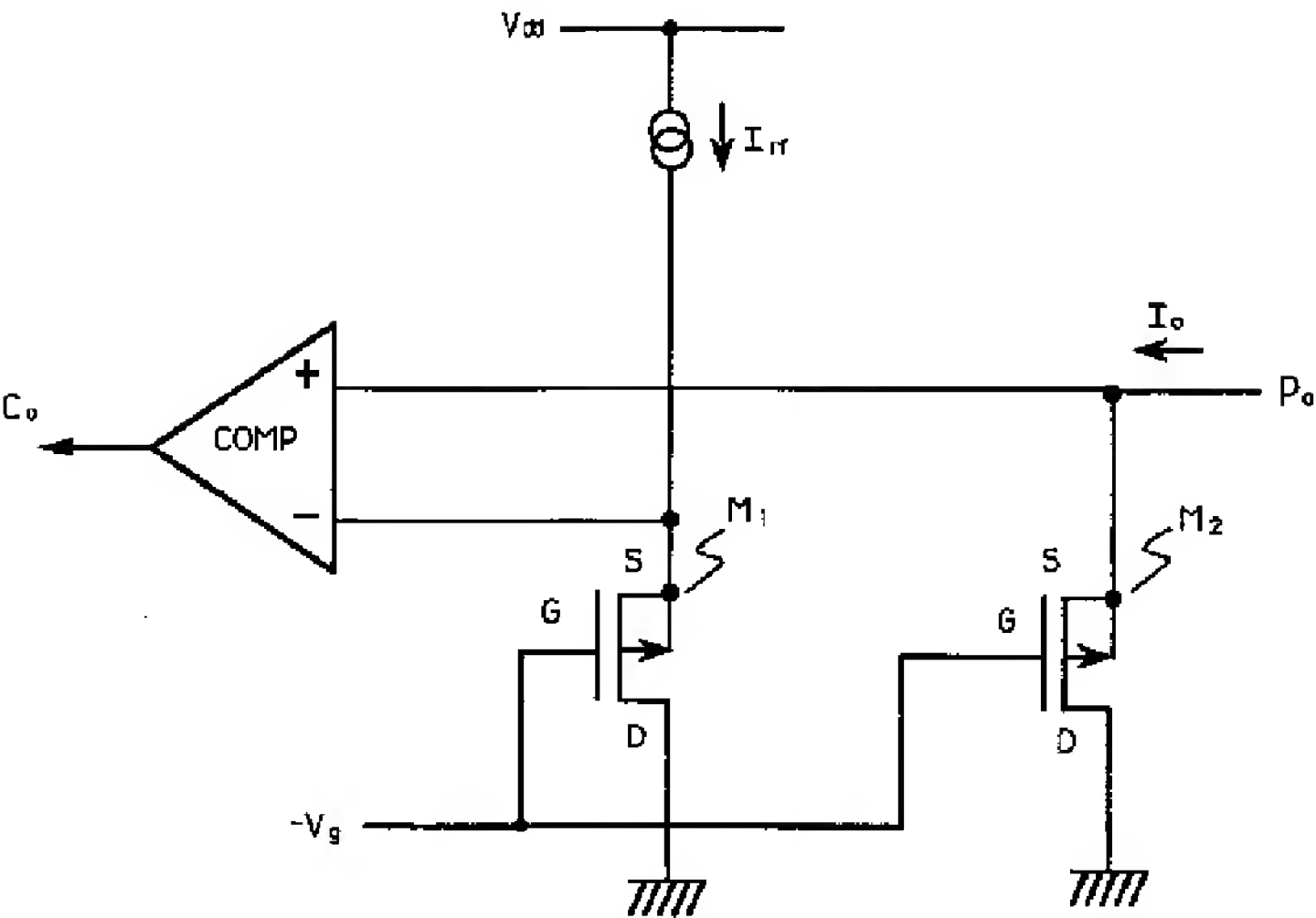


Drawing 4



Drawing 5

50



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1/56	3 1 0		1/56	3 1 0 P

請求項の数 1 (全 5 頁)

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		審査官	橋口 信宏
		(56) 参考文献	特開 平3-75572 (J P, A) 特開 平3-186770 (J P, A) 特開 昭62-247288 (J P, A)

(54) 【発明の名称】 電流検出回路

1

(57) 【特許請求の範囲】

【請求項1】 複数のF E Tトランジスタを用いた電流検出回路において：

ドレイン電極が共に第1電源に接続され、ゲート電極が共に入力信号端子に接続された第1および第2トランジスタと；

前記第1トランジスタのソース電極と第2電源との間に接続された定電流源と；

一方の入力が前記第1トランジスタのソース電極に接続され、他方の入力が前記第2トランジスタのソース電極および出力端子に接続された電圧比較器と；

を備え、

前記第2トランジスタのソース電極の電位と前記第1トランジスタのソース電極の電位とを比較することによって前記出力端子を流れる出力電流の所定値超過を安定的

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に検出することを特徴とする電流検出回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、電流検出回路に関するものである。より詳細には、パワーMOSFETを用いた回路であって、出力電流が最大許容値を超えたことを検出しMOSFETを遮断する高精度の電流検出回路に関するものである。

【0002】

【従来の技術】 従来、パワーMOSFETを用いた電源用ICやモータドライバ用の電流検出回路として、図1に示すような回路があった。同図に示されるように、電流検出回路10は、モノリシックデバイス内に作った2個の並列nチャネルMOSFETトランジスタM1、M2から成る。第1のトランジスタである検出用MOS

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FETトランジスタM1のドレイン電極は出力電流（負荷電流） I_o を受ける出力端子Poに接続され、ゲート電極は入力信号端子Vqに接続され、ソース電極はモニター抵抗Rmを介してアースに接続されている。第2のトランジスタであるパワーMOSFETトランジスタM2は、トランジスタM1と同様に、ドレイン電極が出力端子Poに接続され、ゲート電極が入力信号端子Vqに接続されている。トランジスタM2のソース電極はアースに直接に接続されている。このように出力電流 I_o を

10 パワー部と検出部とに分割することによって、モニター抵抗Rmを検出用として挿入使用できるようになっている。電流検出回路10はまた、電圧比較器COMPを有する。電圧比較器COMPの非反転入力端子は、第1のトランジスタM1のソース電極とモニター抵抗Rmとの間のノードから電圧Vmを入力する。電圧比較器COMPの反転入力端子は、負極がアースされた基準電圧源の正極から基準電圧Vrfを入力する。

【0003】以下に、電流検出回路10の動作について説明する。一般に、MOSFETのドレイン電流 I_d は、 V_{ds} が V_{gs} に比べて極めて小さい動作領域において

20 は、近似的に次式で表される。

【0004】 $I_d = K \cdot W/L \cdot (V_{gs} - V_{th}) V_{ds}$
ここに、Kは比例定数、 W/L はチャネルの幅対長さ、 V_{gs} はゲートソース間電圧、 V_{th} は閾値電圧、 V_{ds} はドレインソース間電圧である。

【0005】モニター抵抗Rmの値が十分小さいと仮定すると、トランジスタM1がオンのときに流れる電流 I_1 によるRmの電圧降下分Vm（ $= I_1 \cdot R_m$ ）の値が、トランジスタM1のドレインソース間オン電圧 V_{ds} に比べて無視できる。この条件が満たされていると、上式において、両FETトランジスタM1、M2の V_{ds} どうしおよび V_{gs} どうしをそれぞれ等しいとみなせる。両トランジスタM1、M2の閾値電圧 V_{th} はほぼ等しいとみなせるので、FETトランジスタM2のドレイン電流 I_2 とFETトランジスタM1のドレイン電流 I_1 との比 I_2/I_1 が、 $I_2/I_1 = (W_2/L_2)/(W_1/L_1) = n$ となり、一定になる。したがってミラー比nが分かっているれば、 I_1 の値を検出することにより、 $I_2 (= n \cdot I_1)$ の値、ゆえに $I_o (= (n+1) \cdot I_1)$ を知ることができる。nの値としてたとえば1000

30 で良い。

【0006】 I_o と I_1 が比例関係にあるとみなせることから、 I_1 によるモニター抵抗Rmの電圧降下分Vmを基準電圧Vrfと比較し（図2参照）、Vmが基準電圧Vrfを越えたことを検出することによって、 I_o が所定値を越えたことを検出することができる。図1の電流検出回路10では、Vmが基準電圧Vrfを越えると、比較器COMPが電流制限信号Coを出力する（図2参照）。電流制限信号Coが出力されることにより、出力電流 I_o が所定の値を越えたことを検出することができ

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る。電流制限信号Coをたとえばゲート電圧Vqを制御する電流制限回路（図示せず）内に入力することによって、ゲート電圧Vqをゼロにし、MOSFETトランジスタM1、M2を遮断することができる。

【0007】上記のように、モノリシックデバイス内でオン抵抗が整合されたMOSFET間を流れる分割電流は比較的良好な固有精度をもっているため、パワーMOSFET電流検出回路10は、ある程度効率良くパワー調整回路等の負荷電流の測定を可能にする。モニター抵抗Rmが検出部トランジスタM1のオン抵抗の10パーセント以下であれば、Rmを無視することができ、検出する電流 I_1 は、ほぼ出力電流/電流ミラー比、つまり I_2/n になる。

【0008】

【発明が解決しようとする課題】しかしながら、実際には、検出損失を低く抑えるために検出部トランジスタM1のチャネル幅 W_1 をトランジスタM2の W_2 に比べて小さく（ $W_1 \ll W_2$ ）設計しなければならず、その場合にトランジスタM1のオン抵抗に比べてRmを無視できる程度に小さくすると、検出用抵抗Rmで発生した検出用電圧では通常、比較器等を含む電流制限回路をドライブするには不十分となる。従って、Rmにはある程度大きな値を使用せざるを得なくなり、Rmを無視できなくなる。すると、検出（ミラー）側の合計抵抗がかなり膨れ上がり、電流ミラー比が変わってしまうという問題点がある。すなわち、Rmを無視できないと、トランジスタM1とM2とのドレインソース間電圧 V_{ds} が互いに等しくなくなってしまい、これにより電流ミラー比が狂ってしまう検出精度が悪くなる。

【0009】本発明は、上記のような問題点に鑑み、検出精度の高い電流検出回路を提供することを目的としている。

【0010】本発明の他の目的は、モニター回路において出力電流を利用せずに、検出損失のない電流検出回路を提供することである。

【0011】

【課題を解決するための手段】上記目的を達成するために、本発明における複数個のFETトランジスタを用いた電流検出回路30は、ドレイン電極が共に第1電源Vddに接続され、ゲート電極が共に入力信号端子Vqに接続された第1および第2トランジスタM1、M2と；

第1トランジスタM1のソース電極と第2電源（アース）との間に接続された定電流源 I_{rf} と；一方の入力が第1トランジスタM1のソース電極に接続され、他方の入力が第2トランジスタM2のソース電極および出力端子に接続された電圧比較器COMPと；を備え、第2トランジスタM2のソース電極の電位と第1トランジスタM1のソース電極の電位とを比較することによって出力端子を流れる出力電流 I_o の所定値超過を検出することを特徴とするものである。

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【0012】

【作用】上記のように構成した本発明の電流検出回路においては、両トランジスタM1、M2の両ソース電位V1、V2がちょうど等しい($V1 = V2$)ときに、両トランジスタのドレイン電流の比 $I2/I1$ が、 $I2/I1 = (W2/L2)/(W1/L1) = n$ (ミラー比)となるように動作する。定電流源I_{ref}によりI₁は所定の値をとるため、出力電流 $I_o = I2$ が最大許容電流値 I_{mx} を越えて流れると、 $I2 > I1 \cdot n$ となる。するとV₂が低下し $V1 > V2$ となり、それを検出した比較器COMPが、電流制限信号C_oを出力する。

【0013】

【実施例】以下に本発明の実施例について図面を参照して説明する。図3は、本発明の一実施例である電流検出回路の構成を示す。同図に示されるように、電流検出回路30は、モノリシックデバイス内に作った2個の並列nチャネルMOSFETトランジスタM1、M2から成る。トランジスタM1、M2は、図5に示すような回路構成によりpチャネルを使用しても良く、他の形式のMOSFETであっても良い。第1のトランジスタである検出用MOSFETトランジスタM1のドレイン電極は電源電圧ラインV_{dd}に接続され、ゲート電極は入力信号端子V_qに接続され、ソース電極は定電流源I_{ref}を介して第2電源であるアースに接続されている。第2のトランジスタであるパワーMOSFETトランジスタM2は、トランジスタM1と同様に、ドレイン電極が電源電圧ラインV_{dd}に接続され、ゲート電極が入力信号端子V_qに接続されている。トランジスタM2のソース電極は出力電流(負荷電流)I_oを取り出す出力端子P_oに接続されている。このように本発明においては、出力電流I_oをパワー部と検出部とに分割していない。そのため、検出部が出力側に影響を及ぼさなくなっている。電流検出回路30はまた、電圧比較器COMPを有する。電圧比較器COMPの非反転入力端子は、第1のトランジスタM1のソース電極と定電流源I_{ref}との間のノードから電圧V₁を入力する。電圧比較器COMPの反転入力端子は、出力端子P_oから電圧V₂を入力する。電圧比較器COMPは、その反転入力値が非反転入力値より小さくなると、電流制限出力信号C_oを出力する。

【0014】以下に、電流検出回路30の動作について説明する。動作の説明のために、両トランジスタM1、M2の両ソース電位V₁、V₂を互いに等しい($V1 = V2$)ものと仮定する。このとき、電圧比較器COMPは電流制限信号C_oを出力しない。一般にMOSFETのドレイン電流I_dは、V_{ds}がV_{qs}に比べて極めて小さい動作領域においては、前掲と同様に次式で表される。

【0015】 $I_d = K \cdot W/L \cdot (V_{qs} - V_{th}) V_{ds}$
上記仮定($V1 = V2$)により、両トランジスタM1、M2のドレインソース間電圧V_{ds}どうしおよびゲートソ

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ース間電圧V_{qs}どうしがそれぞれ等しい。両トランジスタM1、M2の閾値電圧V_{th}はほぼ等しいとみなせるので、FETトランジスタM2のドレイン電流I₂とFETトランジスタM1のドレイン電流I₁との比 $I2/I1$ は、 $I2/I1 = (W2/L2)/(W1/L1) = n$ となる。このようにミラー比nにしたがって動作しているものとする、I₁の値を知ることにより、I₂($= n \cdot I1$)の値、ゆえにI_o($= I2 = n \cdot I1$)を知ることができる。nの値としてたとえば1000で良い。

【0016】このように両ソース電位V₁、V₂が等しいときは、I_oとI₁の比例関係が成り立っている。ところが、実際には定電流源I_{ref}によりI₁は所定の値をとる。出力電流I_o、すなわちI₂の最大許容電流値をI_{mx}とし、定電流源I_{ref}の電流値をI_{mx}/nと設定しておく。そうすることにより、I₂がI_{mx}を越えて流れたとき、I₁はI_{ref}($= I_{mx}/n$)のままであることから、 $I2 > I1 \cdot n$ となる。すると $I2 = n \cdot I1$ の比例関係が崩れ、V₂が低下し $V1 > V2$ となる。それを検出した比較器COMPが、電流制限信号C_oを出力する(図4参照)。したがって、電流制限信号C_oが出力されたことによって、I_oがI_{mx}を越えたことを検出することができる。電流制限信号C_oをたとえばゲート電圧V_qを制御する電流制限回路(図示せず)に出力することによって、ゲート電圧V_qをゼロにし、MOSFETトランジスタM1、M2を遮断することができる。

【0017】

【発明の効果】本発明は、上述のとおり構成されているので、従来技術で経験したようなモニター抵抗R_mによる検出誤差を回避することができ、高い精度でかつ効率良く負荷電流の検出/制限を可能にするという効果が得られる。また、モニター回路での検出用電流I₁は定電流源I_{ref}から供給されており、出力電流I_oの一部を利用するわけではないので、I_oに影響を与えず、効率・精度が良く、さらに適当な安定化回路の設計も容易であり回路の使用条件による影響も受けにくいなど、多大の効果がある。

【図面の簡単な説明】

【図1】従来の電流検出回路を示す。

【図2】図1の回路の動作を説明するグラフである。

【図3】本発明の一実施例にしたがった電流検出回路を示す。

【図4】図3の回路の動作を説明するグラフである。

【図5】本発明の他の実施例にしたがった電流検出回路を示す。

【符号の説明】

30 電流検出回路

V_{dd} 電源電圧V_q 入力信号電圧

M1 第1トランジスタ

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M2 第2トランジスタ

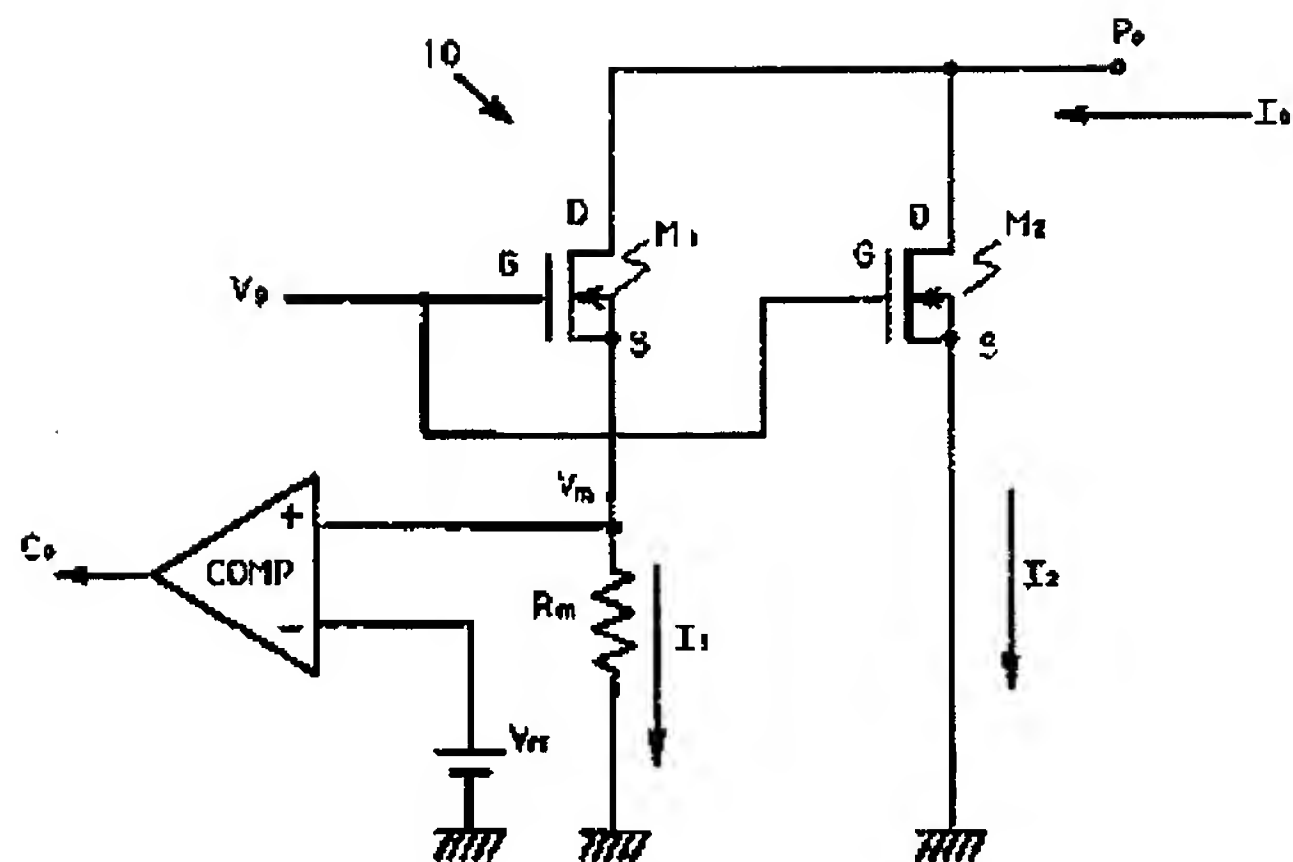
I_{ref} 定電流源P_o 出力端子

*COMP 電圧比較器

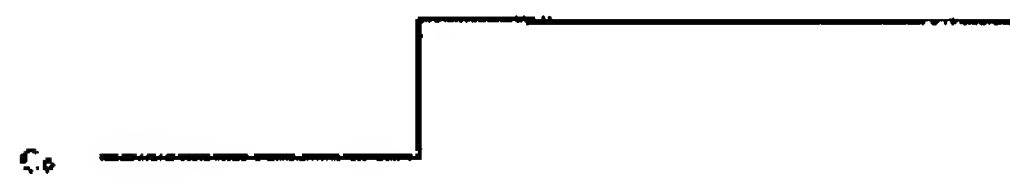
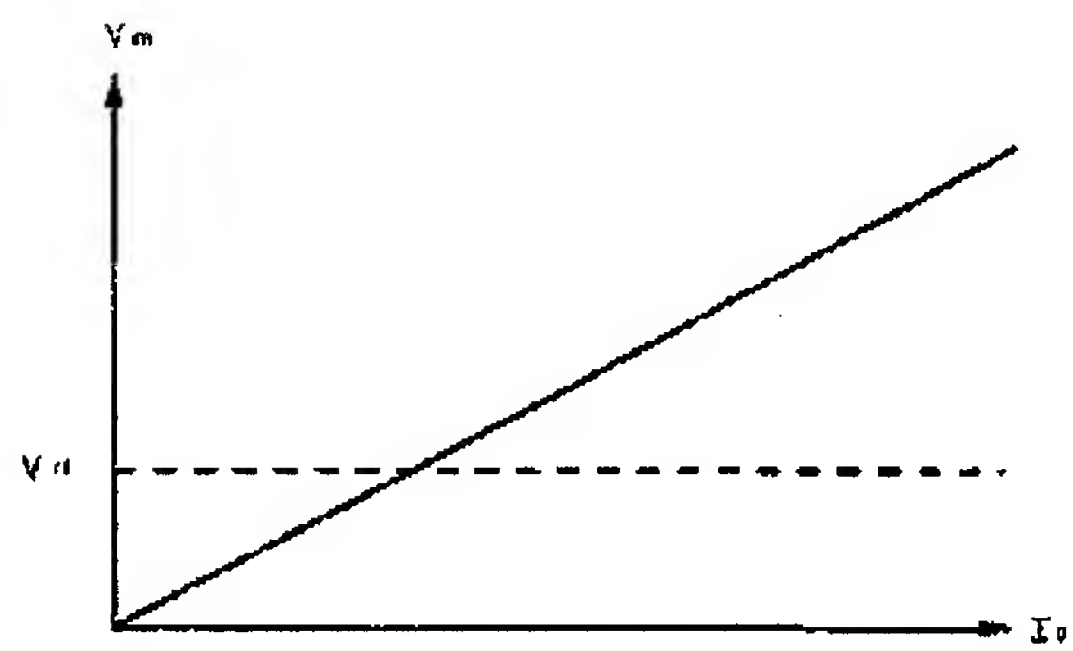
I_o 出力電流

*

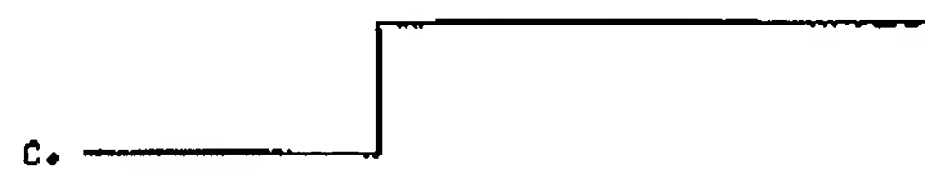
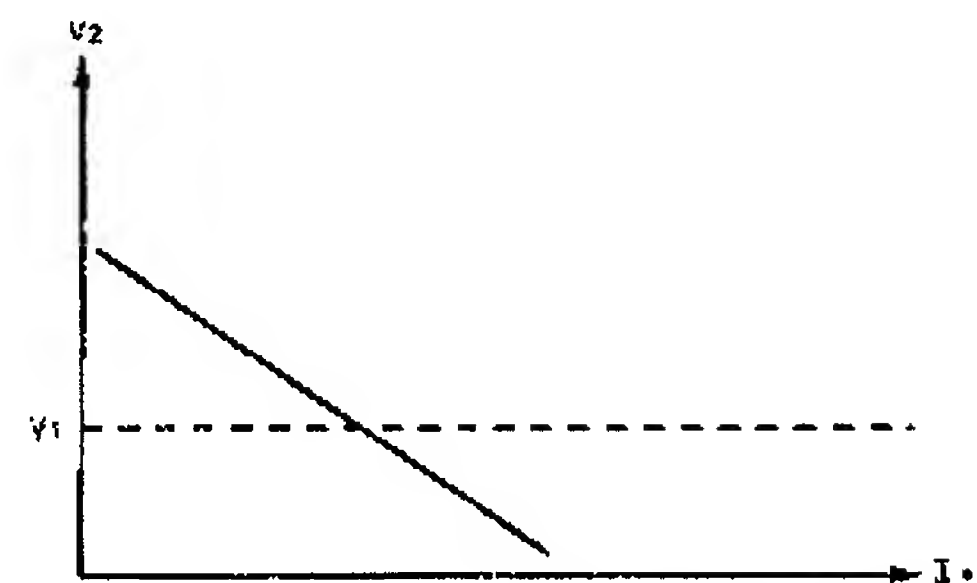
【図1】



【図2】



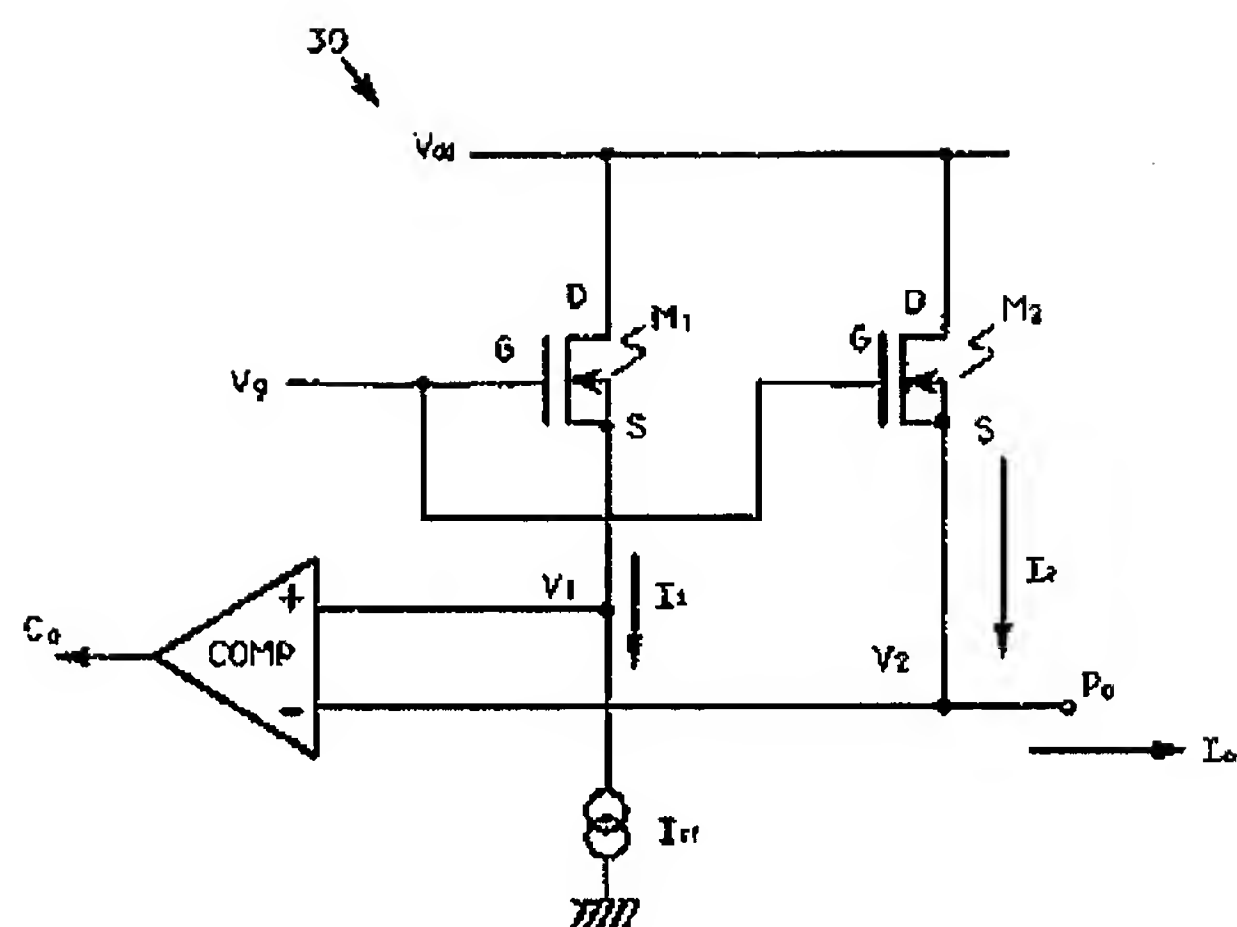
【図4】



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【例3】



【图5】

